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AMENDMENTS TO CLAIMS

Claims 1, 16 and 17 are being amended, claims 4-15 and 18-28 are being canceled, and new claims 29-46 are being added, as shown below. All pending claims are reproduced below, including those that remain unchanged.

1. (Currently Amended) A power control system for controlling the output of a laser diode, comprising:

a write strategy generator adapted to select a desired output from a plurality of different possible desired outputs;

a detector circuit adapted to detect at least a portion of the output of the laser diode and to produce a measured output therefrom;

a comparator adapted to compare ~~a~~ the selected desired output to the measured output, and to produce an error signal therefrom;

an integrator circuit adapted to integrate the error signal, and to produce an integrated error signal therefrom; and

at least one digital-to-analog converter (DAC) adapted to use the integrated error signal to produce a current drive signal that drives the laser diode.

2. (Previously Presented) The system of claim 1, wherein the at least one DAC comprises a READ DAC that converts the integrated error signal to the current drive signal.

3. (Previously Presented) The system of claim 1, wherein the at least one DAC comprises a WRITE DAC that adjusts a write current input based on the integrated error signal.

4.-15. (Canceled)

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16. (Amended) A method for controlling the output of a laser diode, comprising:

(a) selecting a desired output from a plurality of different possible desired outputs;

(b)~~(a)~~ detecting at least a portion of the output of the laser diode and producing a measured output therefrom;

(c)~~(b)~~ producing an error signal based on a comparison between a the selected desired output and the measured output;

(d)~~(c)~~ integrating the error signal to produce an integrated error signal; and

(e)~~(d)~~ using the integrated error signal to produce a current that drives the laser diode.

17. (Amended) The method of claim 16, further comprising repeating steps (a) through (e)~~(d)~~ a plurality of times.

18.-28. (Canceled)

29. (New) The system of claim 1, wherein:

the integrated error signal comprises a count value;

the integrator circuit comprises

an up-down counter adapted to adjust the count value, up or down, based on the error signal; and

a variable rate clock adapted to provide a clock signal to the up-down counter, wherein an adjustable speed of the clock signal specifies a speed at which the up-down counter counts; and

the at least one DAC is adapted to use the count value to produce the current drive signal that drives the laser diode.

30. (New) The system of claim 29, wherein the up-down counter counts down when the error signal indicates that the measured output is greater than the desired output, and

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counts up when the error signal indicates that the measured output is less than the desired output.

31. (New) The system of claim 29, further comprising:
a clamp adapted to prevent the count value from exceeding a maximum value.

32. (New) The system of claim 29, wherein the variable rate clock is adapted to receive the error signal and to adjust the speed of the clock signal based on how long the error signal remains in a same state.

33. (New) The system of claim 32, wherein:
the clock signal speeds up when the error signal remains in the same state; and
the clock signal slows down when the error signal changes state.

34. (New) The system of claim 29, wherein the variable rate clock is adapted to receive the error signal and to adjust the speed of the clock signal based on a magnitude of the error signal.

35. (New) The system of claim 29, wherein the variable rate clock is adapted to increase the speed at which the adjusting of the counter value occurs when the error signal remains in a same state, and to decrease the speed at which the adjusting of the counter values occurs when the error signal changes state.

36. (New) The system of claim 29, wherein the variable rate clock is adapted to adjust the speed of the clock signal based on a magnitude of a difference between the desired output and the measured output.

37. (New) The system of claim 29, wherein the speed of the clock signal can be adjusted to adjust the overall bandwidth of the power control system.

38. (New) The system of claim 29, wherein the at least one DAC includes:

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a PMAX DAC that receives the count signal and produces a reference input signal therefrom; and

a WRITE DAC that receives both the reference input and a digital write current input, and produces the current drive signal therefrom.

39. (New) The system of claim 29, wherein the at least one DAC includes:

a READ DAC that receives the count signal and produces the current drive signal therefrom.

40. (New) The system of claim 39, further comprising:

a current amplifier that amplifies the current drive signal before the current drive signal is provided to the laser diode.

41. (New) The system of claim 29, wherein the detector circuit includes:

a photodetector adapted to detect the at least a portion of the output of the laser diode, and to produce a photo-detect current signal therefrom, wherein the photo-detect current signal is used to produce the measured output.

42. (New) The system of claim 1, further comprising:

a desired power register; and

a desired DAC;

wherein the write strategy generator selects the desired output from the plurality of different possible desired outputs by selecting one of a plurality of digital values stored in the desired power register; and

wherein the desired DAC is adapted to provide the selected desired output to the comparator in response to receiving the selected one of the digital values from the desired power register.

43. (New) The method of claim 16, wherein:

the integrated error signal comprises a counter value; and

step (d) comprises adjusting the counter value based on the error signal; and

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step (e) comprises using the counter value to produce the current that drives the laser diode.

44. (New) The method of claim 43, wherein the adjusting at step (d) includes increasing the speed at which the adjusting of the counter value occurs when the error signal remains in a same state; and decreasing the speed at which the adjusting of the counter values occurs when the error signal changes state.

45. (New) The method of claim 43, further comprising repeating steps (a) through (e) a plurality of times.

46. (New) The method of claim 43, wherein the adjusting at step (d) includes:

increasing the speed at which the adjusting of the count value occurs, when the magnitude of a difference between the desired output and the measured output increases; and

decreasing the speed at which the adjusting of the count value occurs, when the magnitude of the difference between the desired output and the measured output signal decreases.

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